What is claimed is:

1. A metal-insulator-metal (MIM) capacitor comprising:

a first wiring layer and a second wiring layer which are formed on a substrate to be insulated from each other and to which a first voltage and a second voltage are respectively applied;

a lower electrode whose level is higher than the first and second wiring layers and which is insulated from the first wiring layer and contacts the second wiring layer; and

an upper electrode which overlaps the lower electrode with a dielectric layer formed therebetween and contacts the first wiring layer.

2. The MIM capacitor of claim 1, wherein the dielectric layer partially covers the top surfaces of the first and second wiring layers, the upper electrode contacts the first wiring layer through a contact hole that is formed through the dielectric layer to expose the first wiring layer, and the lower electrode directly contacts the second wiring layer.

3. The MIM capacitor of claim 1 or 2, wherein the top surfaces of the first and second wiring layers are planarized.

4. The MIM capacitor of claim 3, wherein the first and second wiring layers comprise:

a barrier metal layer which is formed on the inner walls and bottom surface of a trench formed in an interlayer dielectric layer on the substrate; and

a planarized conductive layer which is formed on the barrier metal layer to bury the trench.

5. The MIM capacitor of claim 3, wherein the first and second wiring layers are wiring patterns embedded in a planarized interlayer dielectric layer which is located

over a lower interlayer dielectric layer formed on the substrate.

6. The MIM capacitor of claim 2, wherein the first and second wiring layers are wiring patterns formed on a lower interlayer dielectric layer formed on the substrate, the lower electrode is formed on the lower interlayer dielectric layer and directly contacts the second wiring layer, and the lower electrode and the first wiring layer are insulated from each other by the dielectric layer.

7. The MIM capacitor of claim 1, wherein the first and second wiring layers are damascene wiring layers which comprise: a barrier metal layer which is formed on the inner walls and bottom surface of a trench formed in a first interlayer dielectric layer on the substrate; and a planarized conductive layer which is formed on the barrier metal layer to bury the trench, the lower electrode is formed on a second interlayer dielectric layer formed on the first interlayer dielectric layer and contacts the second wiring layer through a contact hole that is formed through the second interlayer dielectric layer to expose the second wiring layer, the dielectric layer is formed on the second interlayer dielectric layer and the lower electrode, and the upper electrode is contacts the first wiring layer through a contact hole that is formed through the dielectric layer and the second interlayer dielectric layer to expose the first wiring layer.

8. The MIM capacitor of claim 1, wherein the first and second wiring layers are wiring patterns embedded in a planarized interlayer dielectric layer formed on a lower interlayer dielectric layer formed on the substrate, the lower electrode is formed on an interlayer dielectric layer formed on the planarized interlayer dielectric layer and contacts the second wiring layer through a contact hole that is formed through the interlayer dielectric layer to expose the second wiring layer, the dielectric layer is formed on the interlayer dielectric layer and the lower electrode, and the upper electrode contacts the first wiring layer through a contact hole that is formed through the dielectric layer and the interlayer dielectric layer to expose the first wiring layer.

9. The MIM capacitor of claim 1, wherein the first and second wiring layers are wiring patterns formed on a lower interlayer dielectric layer formed on the substrate, the lower electrode is formed on an interlayer dielectric layer formed on the entire surface of the substrate with the wiring patterns formed thereon and contacts the second wiring layer through a contact hole that is formed through the interlayer dielectric layer to expose the second wiring layer, the dielectric layer is formed on the interlayer dielectric layer and the lower electrode, and the upper electrode contacts the first wiring layer through a contact hole that is formed through the dielectric layer and the interlayer dielectric layer to expose the first wiring layer.

10. A MIM capacitor comprising:

a first wiring layer to which a first voltage is applied;

a lower electrode whose level is higher than the first wiring layer and which is insulated from the first wiring layer; and

an upper electrode which overlaps the lower electrode with a dielectric layer interposed therebetween and contacts the first wiring layer.

11. The MIM capacitor of claim 10, wherein the dielectric layer covers the top surfaces of the first wiring layer and the lower electrode, the upper electrode contacts the first wiring layer through a contact hole that is formed through the dielectric layer to expose the first wiring layer, and the lower electrode contacts a second wiring layer to which a second voltage is applied and whose level is higher than the upper electrode through a contact hole that is formed through an upper interlayer dielectric layer and the dielectric layer to expose the lower electrode, wherein the upper interlayer dielectric layer is formed to cover the upper electrode.

12. The MIM capacitor of claim 10 or 11, wherein the top surface of the first wiring layer is planarized.

13. The MIM capacitor of claim 12, wherein the first wiring layer comprises:

a barrier metal layer which is formed on the inner walls and bottom surface of a trench formed in an interlayer dielectric layer on the substrate; and

a planarized conductive layer which is formed on the barrier metal layer to bury the trench.

14. The MIM capacitor of claim 12, wherein the first wiring layer is a first wiring pattern embedded in a planarized interlayer dielectric layer formed on a lower interlayer dielectric layer formed on the substrate.

15. The MIM capacitor of claim 10, wherein the first wiring layer is a wiring pattern formed on a lower interlayer dielectric layer formed on the substrate, the lower electrode is formed on an interlayer dielectric layer formed on the entire surface of the substrate with the wiring pattern formed thereon, the dielectric layer is formed on the interlayer dielectric layer and the lower electrode, the upper electrode contacts the first wiring layer through a contact hole that is formed through the dielectric layer and the interlayer dielectric layer to expose the first wiring layer, and the lower electrode contacts a second wiring layer to which a second voltage is applied and whose level is higher than the upper electrode through a contact hole that is formed through an upper interlayer dielectric layer and the dielectric layer to expose the lower electrode, wherein the upper interlayer dielectric layer is formed to cover the upper electrode.

16. A MIM capacitor comprising:

a first wiring layer to which a first voltage is applied;

a lower electrode which is insulated from the first wiring layer and whose level is the same as the first wiring layer; and

an upper electrode which overlaps the lower electrode with a dielectric layer interposed therebetween and contacts the first wiring layer.

17. The MIM capacitor of claim 16, wherein the dielectric layer covers the top surfaces of the first wiring layer and the lower electrode, the upper electrode contacts the first wiring layer through a contact hole that is formed through the dielectric layer to expose the first wiring layer, and the lower electrode contacts a second wiring layer to which a second voltage is applied and whose level is higher than the upper electrode through a contact hole that is formed through an upper interlayer dielectric layer and the dielectric layer to expose the lower electrode, wherein the upper interlayer dielectric layer is formed to cover the upper electrode.

18. The MIM capacitor of claim 16 or 17, wherein the top surfaces of the lower electrode and the first wiring layer are planarized.

19. The MIM capacitor of claim 18, wherein the first wiring layer and the lower electrode comprise:

a barrier metal layer which is formed on the inner walls and bottom surface of a trench formed in an interlayer dielectric layer on the substrate; and

a planarized conductive layer which is formed on the barrier metal layer to bury the trench.

20. The MIM capacitor of claim 18, wherein the first wiring layer and the lower electrode are patterns embedded in a planarized interlayer dielectric layer formed on a lower interlayer dielectric layer formed on the substrate.

21. The MIM capacitor of claim 16, wherein the first wiring layer and the lower electrode are patterns formed on a lower interlayer dielectric layer formed on the substrate, the dielectric layer is formed on the entire surface of the substrate with the patterns formed thereon, the upper electrode contacts the first wiring layer through a contact hole that is formed through the dielectric layer to expose the first wiring layer,

and the lower electrode contacts a second wiring layer to which a second voltage is applied and whose level is higher than the upper electrode through a contact hole that is formed through an upper interlayer dielectric layer and the dielectric layer to expose the lower electrode, wherein the upper interlayer dielectric layer is formed to cover the upper electrode.

22. An integrated circuit chip comprising the MIM capacitor of any of claims 1, 10, and 16.